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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,601	12/29/2003	Dong Yeal Keum	SUN-DA-128T	6479

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EXAMINER	
JEFFERSON, QUOVAUNDA	

ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
06/26/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/747,601	KEUM, DONG YEAL	
	Examiner	Art Unit	
	QUOVAUNDA JEFFERSON	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al, US Patent 6,931,980 (as cited in the previous Office Action), in view of Kwon et al, US Patent Application Publication 2003/0045061.

Regarding claim 1, Wu teaches a method for fabricating a transistor comprising of forming a gate electrode **310** on a semiconductor substrate, forming a first preliminary source/drain region **316/318** and a pocket junction region **324/326** through a first ion implantation process using the gate electrode as a mask, the pocket junction region being formed under the first preliminary source/drain region (figures 13 and 14), forming a first oxide layer **328** on the substrate including the gate electrode, forming a nitride layer **330** on the first oxide layer, forming a second oxide layer **332** over the nitride layer (figure 17), forming spacers on sidewalls **334/336** of the gate electrode, forming a second preliminary source/drain region **344** through a second ion implantation process using the spacers as a mask and removing the nitride layer and the first oxide

layer on the surface of the substrate such that the nitride layer and the first oxide layer remain on the substrate only below the spacers after forming the second preliminary source/drain region through the second ion implantation process using the spacers as a mask (figure 21).

Wu fails to teach removing the nitride layer and the first oxide layer on the surface of the substrate after forming the second preliminary source/drain region through the second ion implantation process using the spacers as a mask and diffusing substantially all of the implanted ions in a horizontal direction of the substrate by performing a thermal treatment process for the resulting substrate.

Kwon teaches removing the nitride layer **200** and the first oxide layer **161** on the surface of the substrate (figure 10) after forming the second preliminary source/drain region **230** through the second ion implantation process using the spacers **215** as a mask (figures 7-9) by teaching the use of a series of insulation layers that are deposited over the substrate, including the gate electrode, to form a spacer layer. The top insulation layers are formed into spacer while the two bottom insulation layers remain on the surface of the substrate during the second source/drain implantation process to prevent crystalline defect and ion channeling from occurring during the second high concentration ion-implantation process. After this process, since they are unnecessary, the first and second insulation are etched off the top surface of source/drain region and diffusing substantially all of the implanted ions in a horizontal direction of the substrate

by performing a thermal treatment process for the resulting substrate [0042-0045] by teaching the performance of an annealing process, which not only diffused ion implantations performed in the substrate, the annealing process is also performed to recrystallize damage to the substrate during the ion implantation process

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kwon with that of Wu because the two bottom insulation layers remain on the surface of the substrate during the second source/drain implantation process to prevent crystalline defect and ion channeling from occurring during the second high concentration ion-implantation process. After this process, since they are unnecessary, the first and second insulation are etched off the top surface of source/drain region and by teaching the performance of an annealing process, which not only diffused ion implantations performed in the substrate, the annealing process is also performed to recrystallize damage to the substrate during the ion implantation process

Regarding claim 2, Kwon teaches performing a thermal treatment process prior to the removal of the nitride layer and the first oxide layer [0044-0045].

Response to Arguments

Applicant's arguments, see After Final Response, filed May 15, 2008, with respect to the rejection(s) of claim(s) 1 and 2 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 6,924,180, issued to Quek, discloses method of forming a pocket implant region after formation of composite insulator spacer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUOVAUNDA JEFFERSON whose telephone number is (571)272-5051. The examiner can normally be reached on Monday through Friday, 7AM to 3:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Fernando L. Toledo/
Primary Examiner, Art Unit 2823

QVJ